What is claimed is:

1. A method of manufacturing flash memory device, comprising the steps of:

(a) sequentially forming a tunnel oxide film, a first polysilicon film and a hard mask film on a semiconductor substrate;

(b) etching the hard mask film, the first polysilicon film, the tunnel oxide film and the semiconductor substrate through a patterning process to form a trench within the semiconductor substrate;

(c) depositing an oxide film to bury the trench and then polishing the oxide film by means of a chemical mechanical polishing process until the hard mask film is exposed;

(d) removing the hard mask film;

(e) implementing a cleaning process so that a protrusion of the oxide film is recessed to an extent that the sidewall bottom of the first polysilicon film is not exposed;

(f) depositing a second polysilicon film on the results in which the protrusion of the oxide film is recessed and then polishing the second polysilicon film until the protrusion of the oxide film is exposed;

(g) forming a dielectric film on the second polysilicon film; and

(h) forming a control gate on the dielectric film.

2. The method as claimed in claim 1, further comprising the steps of: before the tunnel oxide film is formed on the semiconductor substrate,

forming a sacrificial oxide film on the semiconductor substrate;

implementing ion implantation for forming wells and ion implantation for controlling the threshold voltage, using the sacrificial oxide film as a buffer layer; and

removing the sacrificial oxide film.

3. The method as claimed in claim 1, further comprising the step of before the step (g) after the step (f), implementing a cleaning process for recessing the oxide film between the second polysilicon films by a given depth in order to increase a contact surface area of the second polysilicon film and the dielectric film.

4. The method as claimed in claim 1, wherein the hard mask film is formed using a silicon nitride film having an etch selectivity ratio to the oxide film and is formed in thickness through which the oxide film is protruded sufficiently higher than the surface of the semiconductor substrate.

5. The method as claimed in claim 1, wherein the oxide film is a HDP oxide film and is deposited in thickness that could be deposited higher than the top surface of the hard mask film while completely burying the trench.

6. The method as claimed in claim 1, wherein, the cleaning process for recessing the protrusion of the oxide film employs DHF and SC-1 solution.

7. The method as claimed in claim 1, wherein the first polysilicon film is formed using an amorphous polysilicon film into which a dopant is not doped and wherein the amorphous polysilicon film is formed by means of a low pressure-chemical vapor deposition (LP-CVD) method using SiH_4 or Si_2H_6 gas at a temperature of 480～550℃ and a low pressure of 0.1～3Torr.

8. The method as claimed in claim 1, wherein the second polysilicon film is formed by means of a low pressure-chemical vapor deposition (LP-CVD) method using SiH_4 or Si_2H_6 gas and PH_3 gas at a temperature of 550～620℃ and a low pressure of 0.1～3Torr.

9. The method as claimed in claim 1, wherein the control gate is formed to have a dual structure on which a film into which a dopant is doped and a film into which a dopant is not doped are sequentially stacked, in order to prevent diffusion of fluorine (F) that may be substitutionally solidified into a dielectric film to increase the thickness of the oxide film.

10. The method as claimed in claim 9, wherein the amorphous polysilicon film into which the dopant is doped is formed by a low pressure-chemical vapor deposition (LP-CVD) method using SiH_4 or Si_2H_6 gas and a PH_3 gas at a temperature of 510～550℃ and a pressure of 0.1～3Torr and the amorphous polysilicon film into which the dopant is not doped by an in-situ process after supply of the PH_3 gas is stopped.

11. The method as claimed in claim 1, wherein the dielectric film is formed to have a stack structure on which an oxide film, a nitride film and an oxide film are sequentially stacked.

12. The method as claimed in claim 11, further comprising the step of before the step (h) after the step (g), implementing a steam anneal process at a temperature of 750～800℃ in order to improve the film quality of the dielectric film and enhance the interface between the stack structure of the oxide film, the nitride film and the oxide film.